national accelerator laboratory

TM-360
2610.900

OPERATIONAL DESCRIPTION OF DIGITIZER 22X2140 FOR THE EMI MULTI-WIRE PROPORTIONAL CHAMBERS WITH DELAY-LINE READOUT

F. Kirsten, E. Binnall, K. Lee, and C. Nunnally
Lawrence Berkeley Laboratory

April 20, 1972

Operated by Universities Research Association Inc. Under Contract with the United States Atomic Energy Commission

1.0 PURPOSE

This is a CAMAC module that digitizes the times-of-arrival of up to 16 pulses on each of seven "Data Signal" inputs. The time base is determined by an externally-supplied train of clock pulses. It is designed to be used with delay-line readout of multi-wire proportional chambers, particularly where events occur close together in time.

In its "one-pass" Write mode it can digitize the times-of-arrival within a time base equal to 4096 clock periods. In the "wrap-around" mode, it can digitize within a larger real-time base, where time is measured in clock counts modulo 4096. (See Section 10.)

2.0 BRIEF DESCRIPTION OF OPERATION*

2.1 Digitizing (Write) phase

Each module accepts the following input signals:

a) 1 Write Permit input
b) 1 Clock input (25 MHz max.)
c) 7 Data Signal inputs, numbered 0 to 6.

Signals a) and b) originate in a Clock Generator module; c) signals come from the chamber via the discriminator.

Near the beginning of a digitizing interval (e.g. beam spill), the Write Permit is changed from logic '0' to '1'. This sets the module into the digitizing mode. The external clock may be started soon thereafter. An internal 12-bit scaler counts the clock pulses. "Time" is measured from the start of the clock pulse train. Presumably, each Data Signal input then receives its independent train of signals. At the instant that each Data Signal input changes from '0' to '1', the digitizer records the contents of the scaler. The '1' to '0' transition causes no action. Up to 16 '0' to '1' transitions on each of the seven inputs can be recorded. In the one-pass mode, the clock pulse train stops before, or just as, the scaler is full. Write Permit then goes to '0'. No further digitizations are done after the clock train stops or after Write Permit goes to '0'.

2.2 Readout Phase

2.2.1 Data

The digitized data is readout using the Stop-mode Q-response (see section 5.4.3.3 of CAMAC (72)). Potentially, there are 7x16=112 words of data per module. Generally, only a fraction of these words will have a "fresh" data from the last digitizing spasm. The read logic is such that only the fresh data words are transmitted, each accompanied by Q='1'. The response is Q='0' after all fresh data has been read. If a module has no fresh data, it responds with CAMAC Q='0' on the first word.

*Figure 4 is an organizational block diagram of the digitizer. Full logic diagrams are on 22X2140W1-W10.

2.2.2 Identification

If a module has fresh data, the first word it sends is an I.D. word identifying which module is being read out.

In addition, three bits of each data word indicate from which of the seven channels the current data word comes.

2.3 Resetting

Under normal conditions, the module is ready to digitize as soon as readout is finished, and Write Permit goes to '1'. However, other resetting means are provided, and must be used if the readout phase was not completed, or to initialize the system.

2.4 Testing

The most thorough test consists of pulsing a Data Signal input with a train of pulses accurately timed with respect to a pseudo-Start of Spill Sync, used to start the clock pulser.

Means are also provided for testing nearly all of a module by CAMAC commands. To simulate the digitizing and storage, the scaler can be be loaded with a number, and this number read into any desired channel of storage. Thus, a fairly simple software algorithm can do a fairly complete check of the scaler and read/write memory.

3.0 USE IN A SYSTEM

Figure 1 is a schematic block diagram showing the interconnections between a digitizing module and the rest of the system. The parts above line A-A are concerned with digitizing (writing); those below with data transfer (reading) and control. Three of the seven input channels are shown connected to three discriminators. Two discriminators observe the two ends of one delay line, the third sees a "common" signal. The other four input channels can be used for two other delay lines of the same MWPC.

A separate clock (CAMAC) module feeds Clock pulses and Write Permit signals to many digitizing modules in parallel; only one digitizing module is shown in the block. The parallel distribution of these signals means all digitizers use the same time base. The time base is started by the Start of Spill Sync pulse.

Data transfer and control is via the CAMAC Dataway.

4.0 CONNECTORS AND SIGNAL SPECIFICATIONS

The following connectors are on the front panel: All connectors are LEMO:

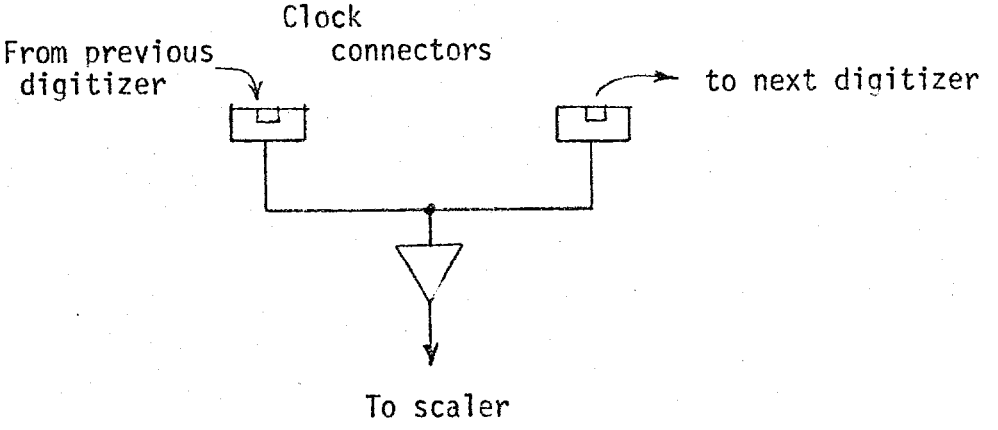
4.1 Two-"Clock" connectors"

"In-out wired with internal tap--permits daisy-chaining the clock signal from module to module. Number of modules

on the chain limited by permissible propagation delays in Clock signal. This propagation delay affects the correlation of data from separate chambers.

*TTL signal levels: Scaler counts the low to high transition;

*Max clock frequency ∿ 25 MHz (40 nsec period)



4.2 Two "Write Permit" connectors

"In-out wired with internal tap. (See 4.1).

Propagation delay not as important here as it is with clock.

*TTL signal levels;

Low level = '1' --, permit digitizing

High level = '0' --, permit reading; digitizing inhibited

*Timing: Should go to '1' approximately 50 nsec before first clock. Should not go to '0' for approximately 100 nsec after last clock.

4.3 Seven "Data Signal" inputs

*TTL signal levels; Low level = '0'; High level = '1'; Unterminated.

*Digitizing is with respect to low to high transition.

*Low to high transitions should be no closer than nsec to be recognized.

*Channels are numbered from 0 to 6.

5.0 SIZE AND POWER

5.1 Size: Double-width CAMAC modules.

5.2 Power required:

+6V @ 4.3 amps. (Later versions may draw 3.5a)

6.0 CAMAC COMMANDS

N·F(0)·A(x)- - -	Read a data word. Sub-address ignored by module. Q=1: This data or I.D. word is valid (Meaningful) Q=0: This data or I.D. word is invalid, and there are no (more) valid data words in this module. A Q=0 on first F(0) addressed to a module means that module has no "fresh" (See 2.2.1) data
N·F(8)	Test Look-at-Me (L) Q=1 if L=1 Q=0 if L=0
N·F(16)·S1	Load scaler with data carried on Dataway Write lines W1 - W12.
N·F(24)A(0)	Disable Look-at-Me
N·F(24)A(1)	Disable "Internal Write Permit"; test is finished.
N·F(26)A(0)	Enable Look-at-Me
N·F(26)A(1)	Enable "Internal Write Permit in preparation for test routine.
N·F(28)·S2	GRW (Get Ready to Write) Reset Scratch pad memory address register. Used to prepare for test, or if previous readout was not completed.
N·F(30)·A(i)·S2	Load contents of scaler into next available memory location of Channel i, $0 \leq i \leq 6$. Does not indicate if memory is full. Q='1' if $0 \leq i \leq 6$; Q='0' otherwise.
Q response	F(0), F(8), F(30) } See above

L — L='1' if Enabled and if Write Permit = '0' and there is "fresh" (See 2.2) data in memory that has not yet been read out. (L goes to '0' at S2 of cycle reading out first "fresh" word.)

7.0 BIT FORMATS (Numbers correspond to positions in CAMAC data word)

See page 7 for ID word and data word formats.

8.0 WORD SEQUENCE

For reasons only a logic designer could understand, the digitizer reads out words in reverse order according to channel number and times-of-arrival. Thus, the channels are read out in the order 6,5,4,3,2,1,0, and in each channel the number corresponding to the last received Data Signal pulse is read first; the first received is read out last. If the simplest mode of digitizing is used (number of clock pulses $\leq$ 4096) this means that, of the values of data words in a channel, the highest will be read out first, the lowest last. If a wrap-around mode (Sec. 10.2) is employed (number of clock pulses > 4096), this is not necessarily true.

An example is shown in Figure 2 and Table I. Figure 2 shows the input pulse pattern to three digitizers, numbered 5,6, and 7, located in CAMAC stations 10, 12 and 14 (double-width modules). Table I shows the words read on successive CAMAC read cycles.

In the case of the NAL set-up, we expect 7 Data Signal inputs from each of 1 meter^2 chamber. Thus, one digitizer per chamber. Likewise, we would expect approximately the same number of pulses in each channel. The example is purposely slightly spurious to show examples of behavior.

9.0 PROGRAMMING IMPLICATIONS

Note that only the low-order 16 bits of the 24-bit CAMAC word are significant. Thus a 16-bit computer needs one memory location for each data word.

Following a digitizing spasm, each digitizer module will have a variable number of words to be read out. The software must be able to identify the source of each word. As described in 2.2.2 and 7.1, ID words and bits have been provided to facilitate this.

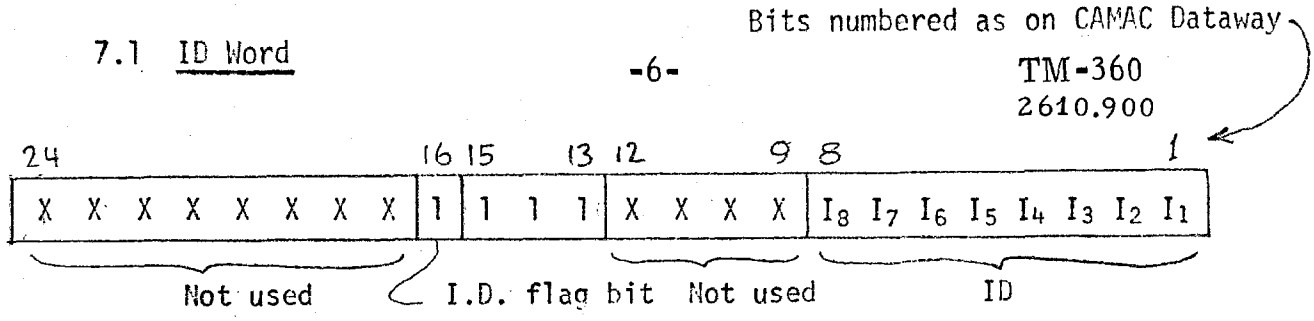
9.1 Transfer of blocks of data from groups of modules.

The Stop-mode Q-response can be interpreted either in hardware or software depending on the capabilities of the CAMAC system controller (i.e. computer interface, whether Crate Controller or Branch Driver).

9.2 Hardware-controlled block transfers via Direct-Memory Access, or Data Channel.

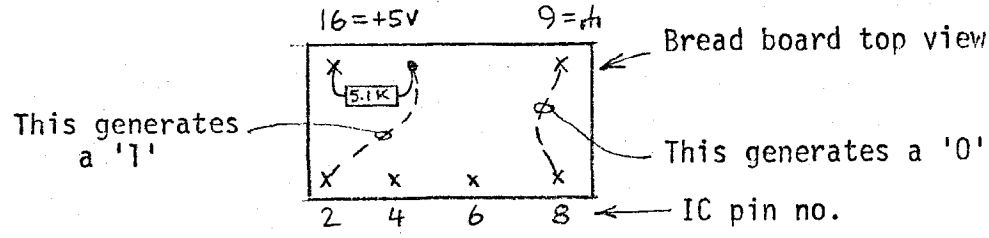
If the system controller has hardware compatible with Stop-mode Q response, the data transfer is accomplished with a minimum of

7.1 ID Word



Bits:	Significance
1-8	- Module ID number. This number is coded by pre-wiring two 16-pin dual-in-line bread-boards in positions P4 and R4 of the module.

$$ID = \sum_{i=1}^{8} I_i \, 2^{i-1} \; ; \; I_i = 0,1$$



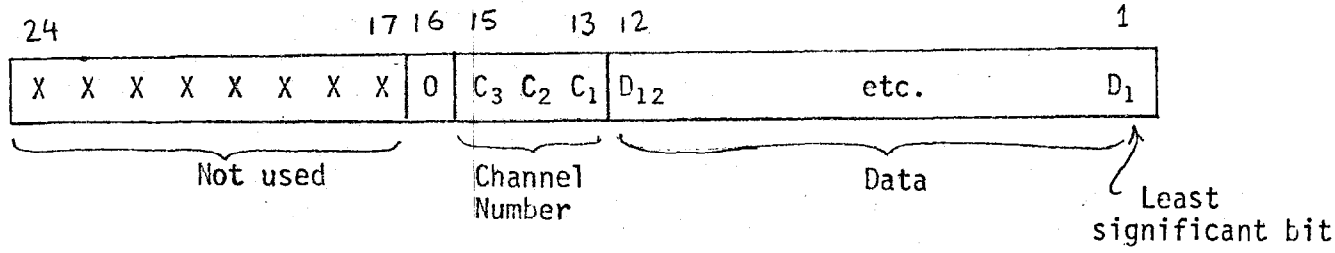
I_1 I_2 I_3 I_4 - - - P4

I_5 I_6 I_7 I_8 - - - R4

13-15 - Generates a 7_8; (not particularly significant)
16 - '1' is flag for ID word

7.2 Data Word.

All valid data words except the ID word have this format.



Bits	Significance
1-12	Data word, 12 bits, binary; Bit 1 is least significant bit
13-15	Channel number; this data word comes from channel j, $0<j<6$, where $j=C_1x1+C_2x2+C_2x4$; $C_i=0,1$
16	Always 0

programming. The algorithm is:

1) Load the controller CAMAC command register with F(0) N(i) A(x)

x means immaterial
i is the station number of the first module in the group

2) Command the controller hardware to do a series of CAMAC cycles.

3) At the end of each cycle, the hardware does the following

a) If the response was Q=1

*Transfer data to computer memory

*Repeat CAMAC cycle at same CAMAC address

b) If the response was Q=0

*Do not transfer data

*Update CAMAC address to:

F(0)·N(i+1)A(x)

*Repeat CAMAC cycle

4) Continue 3) until all CAMAC addresses exhausted.

Note that this scheme is compatible with CAMAC modules, such as scalers, that use the Address Scan mode of Q-response (CAMAC (72), Sec. 5.4.3.1), provided that they have a maximum of 15 registers.

9.3 Programmed block transfers. Two algorithms can be used, one based on Q, one on L.

9.3.1 Q response. This can be derived from the discussion of 9.2 and Table I, except the Q state is examined by software, rather than hardware.

9.3.2 L-flag. At the end of digitization, when Write Permit goes to 0, each module that has "fresh" data and in which the L is enabled will set its L='1'. Thus, depending on the L-sorting hardware available, one could design a routine in which, for example, the computeris interrupted if any L='1'. The interrupt service routine then reads modules until all L flags are '0'. There are many variations possible.

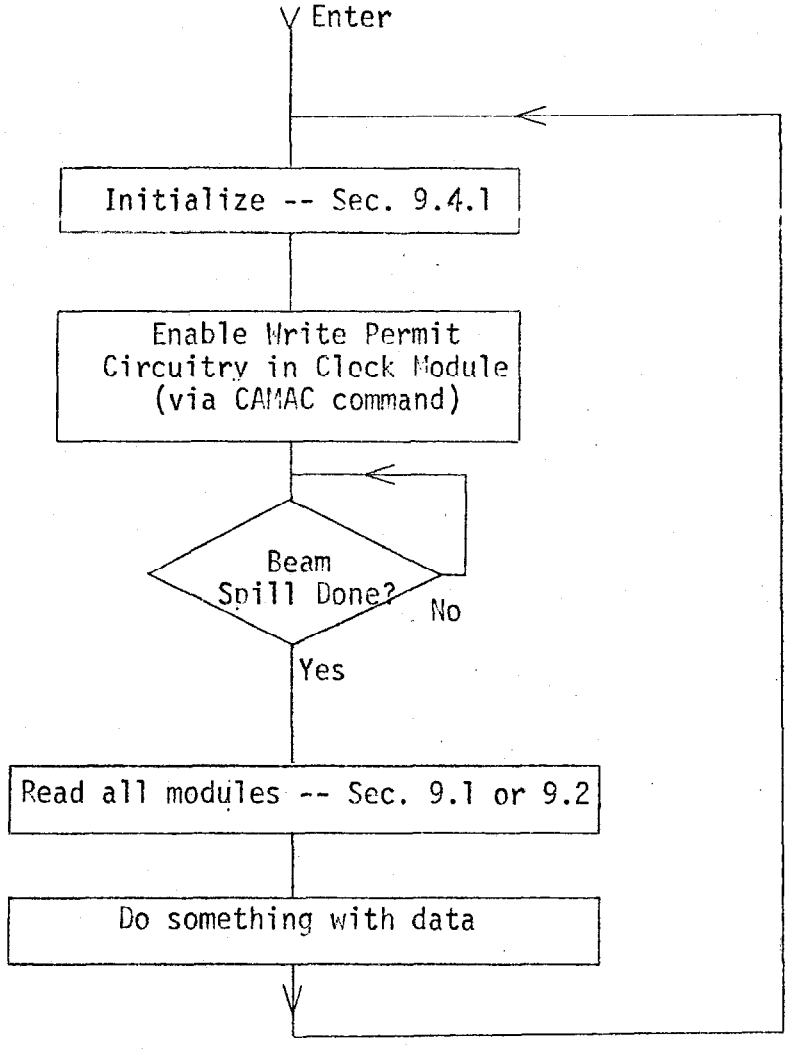
9.4 Complete Sequences

9.4.1 Initializing

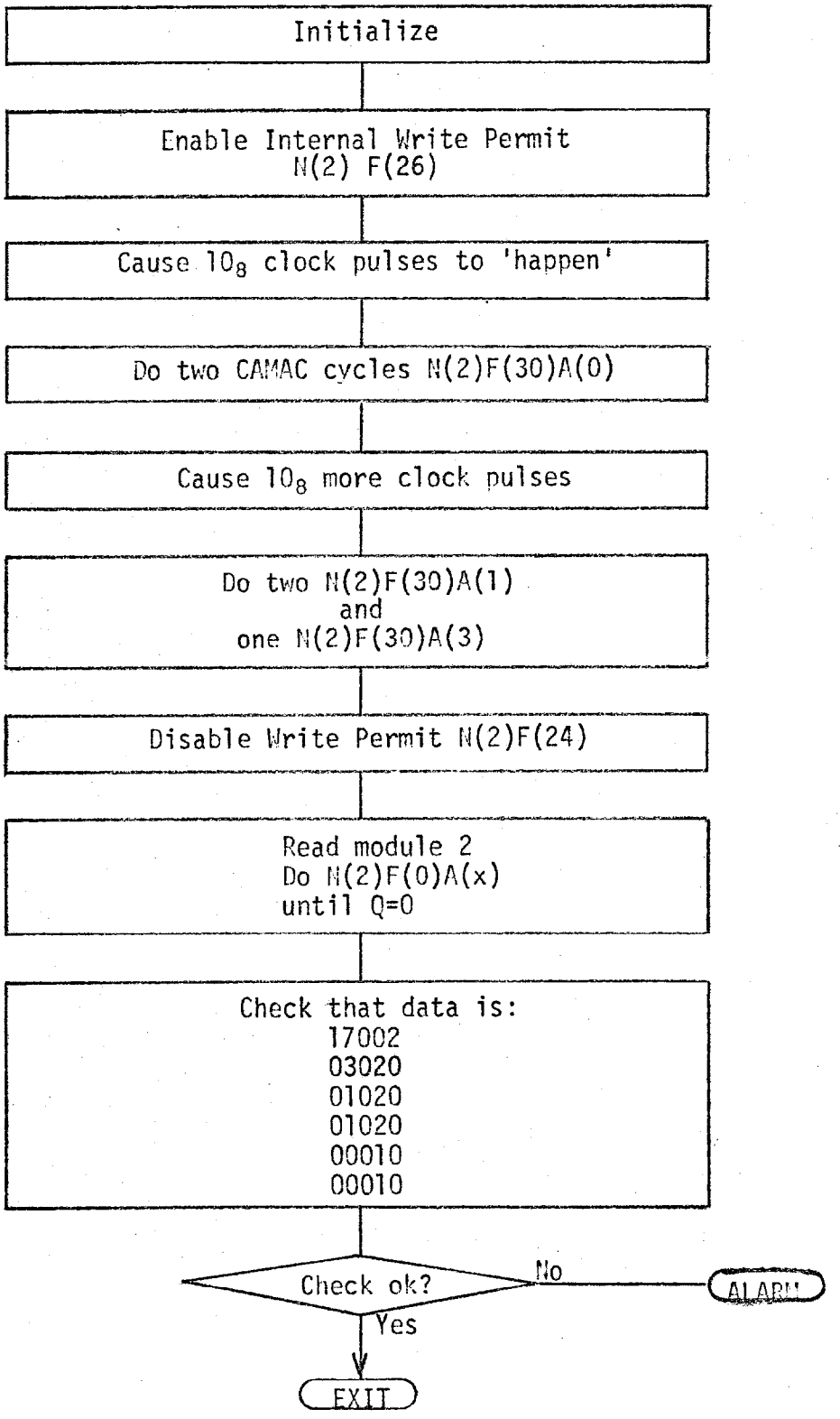
Most of the necessary initializations are done automatically. For example, as long as Write Permit is '0', the clock scaler is clamped in the reset state and Data Signal inputs are gated off.

The address registers for each scratch pad are reset to the correct condition for writing during the process of completely reading out the module. Therefore, if a module is not completely read, these registers must be reset in another way. Two other measures are provided--clear (C) and F(28), GRW. If the crate contains no other modules that are affected by C, this does the job nicely. If C is not usable, do F(28) followed by F(26) addressed to all modules. This can be done in two Dataway cycles if multi-station addressing is used.

9.4.2 A possible sequence:



9.4.3 Test routines: One possible test is illustrated below. The test is performed on the module in station 2.



10.0 MODES OF DIGITIZING

10.1 One-Pass

The 12-bit scaler in each module can count 4096 clock pulses. Thus, it can unambiguously define the time-of-arrival within 4096 time bins (of down to 40 nsec each). The one-pass time base is: 4096 clock periods >163.84 μsec. [If both ends of delay line are read, and velocity propagations =5nsec/mm, the resolution is thus 4 mm].

10.2 Wrap-Around

The module digitizes perfectly well if the clock pulses exceed 4096 in number. Each time the number exceeds N*4096, N=0,1,2--etc., the scaler starts over -- i.e., it counts modulo 4096. If the order in which events occur need not be preserved, this is a usable way to operate, provided of course, no more than 16 events are input to each channel.

Since the scalers in all modules start over on the same clock pulse, there isno loss of time-correlation between modules (chambers).

The programmer needs to be told if wrap-around is used. For example, the signal from one end or the other of a delay line may show up as a very low number. Perhaps it requires a negative number from the other end of delay line and from the prompt pulse to satisy the reconstruction algorithm. This negative number may exist, but manifests itself as a number near 4096. The familiar time-distance diagram in Fig. 3 illustrates this. In the diagram, events A and D are completely contained in scaler pass 1 and 2 respectively while B and C overlap.

Of course, the data as read into computer contains no hint as to which scaler pass was involved. There is only one "virtual" pass of 0 to 4095. Thus, in examining the events shown, the program comes first to an "END B" pulse with a count of ∿ 0002. To reconstruct this event (which we know to be event B, the program needs a negative number for END A and PROMPT. It finds these near 4090.

11.0 NOTES

11.1 Time Relation to Other Modules

The time bases in all digitizing modules are identical to within the relative timing of clock pulses at each module.

11.2 All input pulses arriving between opening of Write Permit and first clock are digitized as '0000_8'.

11.3 Note that wrap-around mode is quite useful in testing with a source or cosmic rays. Keep wrapping around until 16 events are counted, then read out.

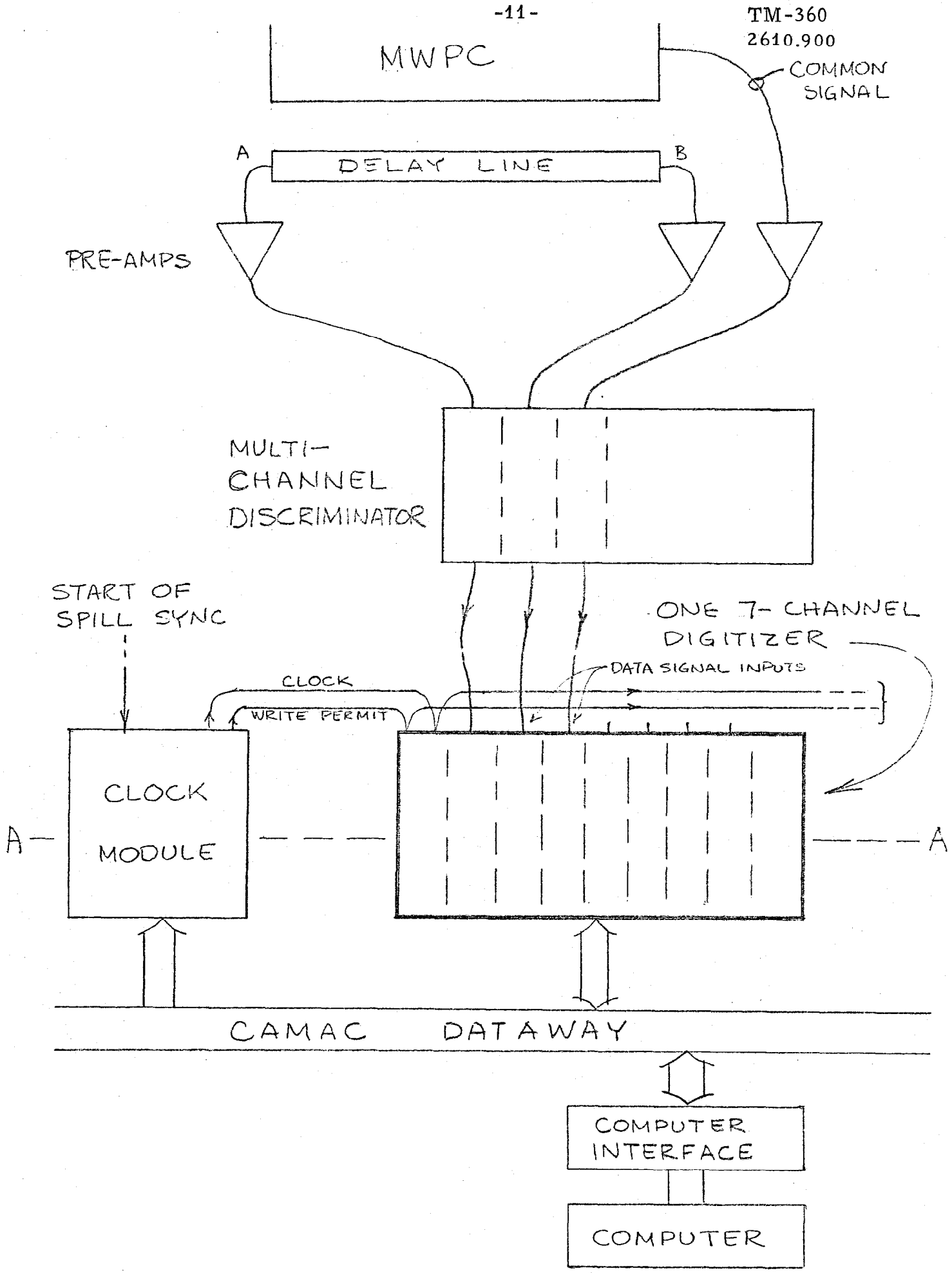
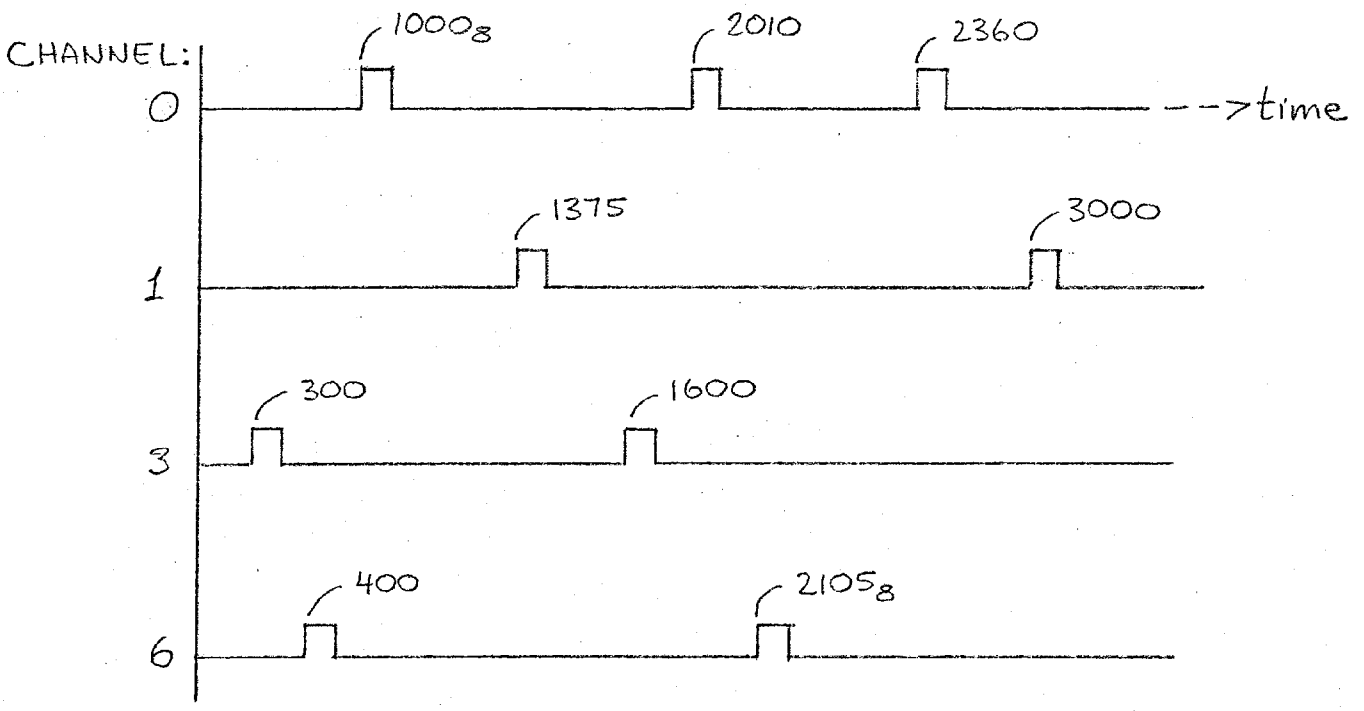


Fig. 1 Relation of digitizer to other system components.

Input pulses to digitizer 5, in station 10



Digitizer 6 in station 12

No pulses received

Digitizer 7 in station 14

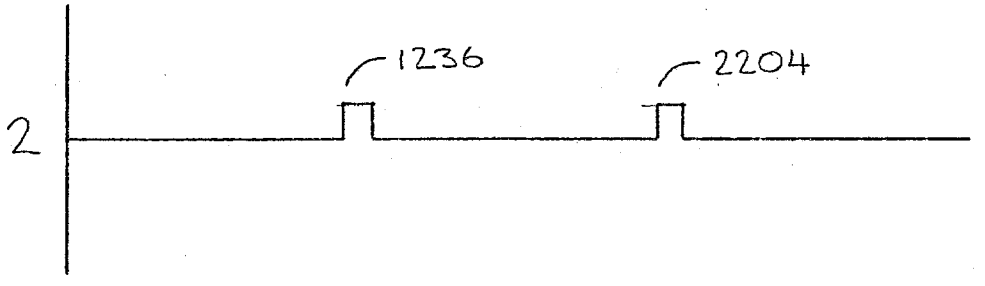


Fig. 2 Input pulse pattern corresponding to data shown in Table I.

TABLE I

CAMAC Cycle	Data read onto Dataway (Octal)	Q	Comments	Action of CAMAC Computer interface Transfer data to core--yes/no	N
1	170005	1	ID word for digitizer 05	Yes	10
2	062105	1	1st data word, channel 6	"	"
3	060400	1	2nd " " " 6	"	"
4	031600	1	1st " " " 3	"	"
5	030300	1	2nd " " " 3	"	"
6	013000	1	1st " " " 1	"	"
7	011375	1	2nd " " " 1	"	"
8	002360	1	1st " " " 0	"	"
9	002010	1	2nd " " " 0	"	"
10	001000	1	3rd " " " 0	"	"
11	000000	0	End of digitizer 05	No	"
12	000000	0	Finds no module in Station 11	No	11
13	000000	0	No fresh data in digitizer 06	No	12
14	000000	0	Finds no module in Station 12	No	13
15	170007	1	ID for digitizer 07	Yes	14
16	022204	1		"	"
17	021236	1		"	"
18	000000	0	End of digitizer 07	No	"

Assumed conditions:

1) Double-width modules, hence digitizer 5 is in station 10, etc.

2) A block transfer mode of reading, in which the CAMAC controller uses the following algorithm for modifying CAMAC addresses:

   if Q=1, A=A+1 for next F(0) command

   if Q=0, A=0, N=N+1 for next F(0)

3) Additional comments

Cycles	Significance
1-10	Read the ID word for module 5 plus 9 data words. Note Q='1' for all ten words.
11	Q=0 shows the last "fresh" data word from module 5 was read on the previous cycle.
12	In the CAMAC address, N has now been advanced to 11. Since no module is in station 11, Q=0.

TABLE I (Cont'd.)

Cycles	Significance
13	N has been advanced to 12. This module (chamber 6) has no data, so Q=0.
14	Similar to cycle 12.
15	ID for chamber 7
16-17	Transfer data
18	No more data

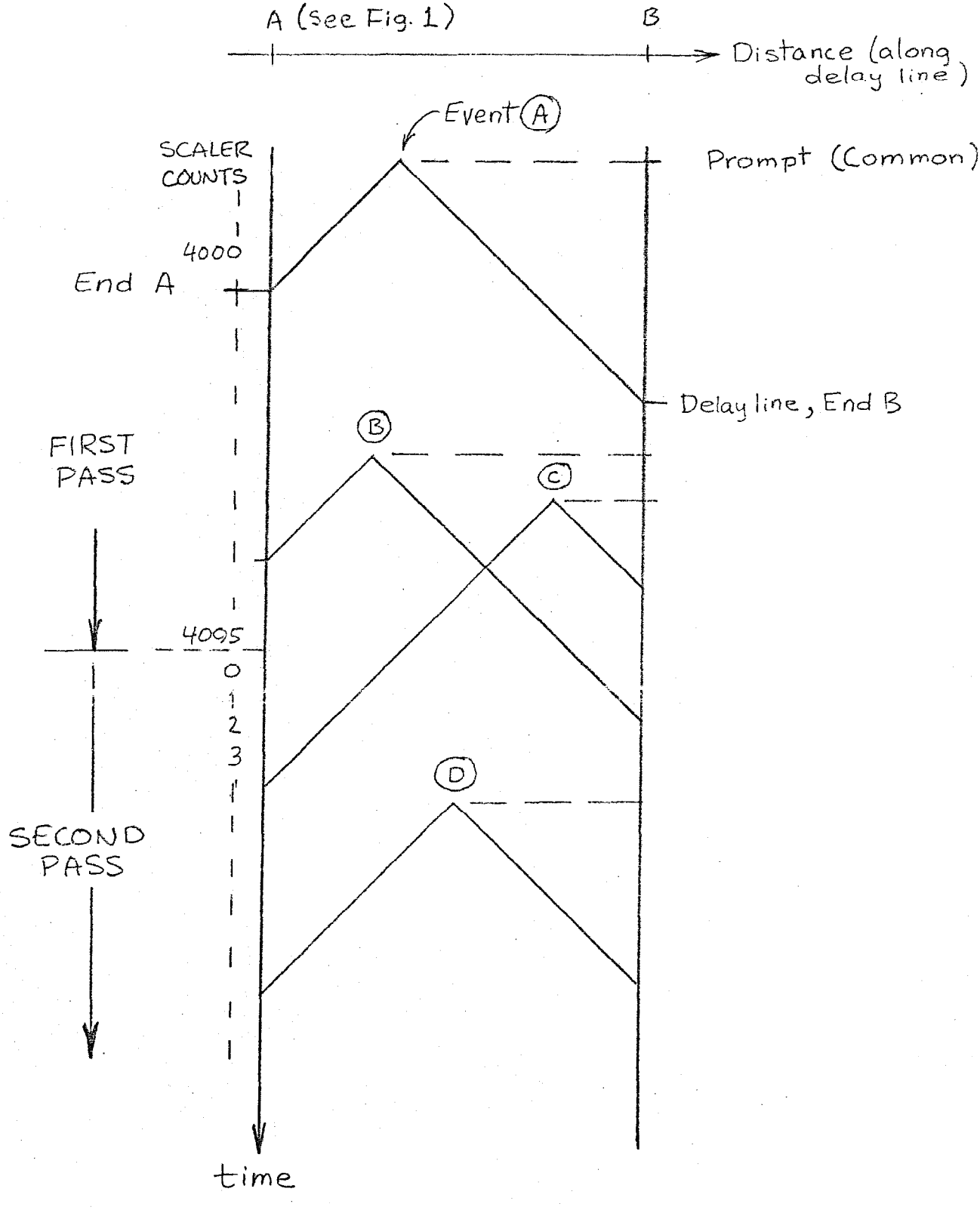


Fig. 3 Time-distance diagram for illustrating wrap-around mode of digitizing.

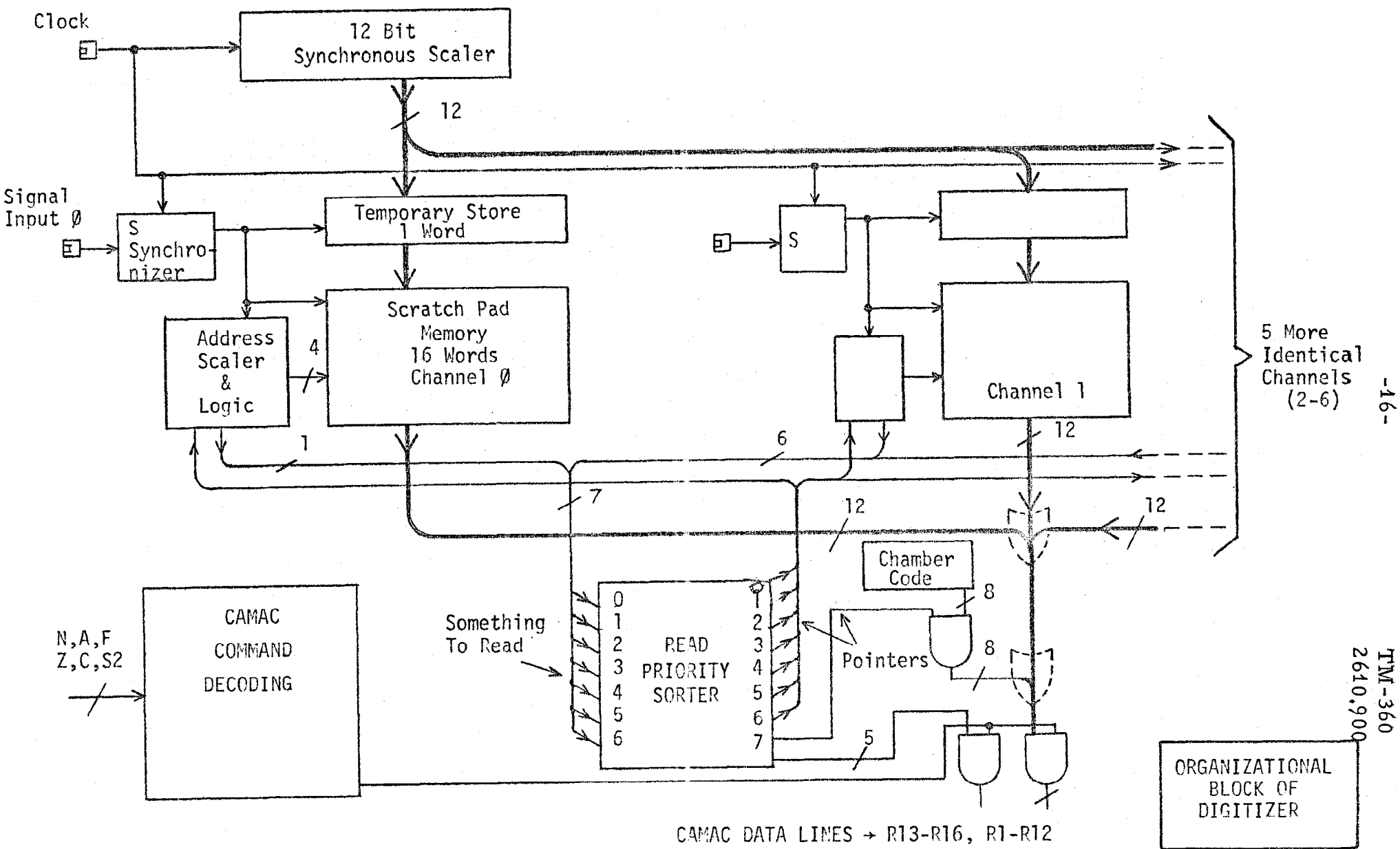


Fig. 4 Full details on prints 22X2140W1-W10

TM-360
2610,900